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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,792	03/17/2004	Nam-Jung Her	4591-363	5596

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,792	HER ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *5,6 and 12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-15 are present for examination.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (03/17/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that no Information Disclosure Statement (IDS) was provided with the application.

Drawings

The drawings filed with this application are accepted since the examiner sees no issues with them at this time

Specification

The abstract of the disclosure is objected to because it is unclear to the examiner if each "In an embodiment" on pages 2-3 lines 24-10 and on page 3 lines 15-29 of the specification are separate inventions or specific embodiments under "According to an aspect of the present invention" on page 2 line 17 and under "According to another embodiment" on page 3 line 11 respectfully. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 5-6 and 12-15 are objected to because of the following informalities:

The claims uses the word "to" in abundance making the claims unclear as per what applicant is referring to.

In claims 5 and 12 the wording "to first to" is unclear in the contexts of the claim.

Appropriate correction is required. Examiner notes any claims dependent on a claim or claims with an objection should be corrected so as to work in conjunction with any corrections made to a claim or claims it is dependent upon.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-6 and 12-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "the (i +1)th output signals" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that only ith output signals have been established within the claim in line 2 of the claim.

As per claims 5 and 6, it is unclear to the examiner how anything if sent "to (N/2)th output signals" in line 2 of the claims. For the purposes of examination the (N/2)th output signals will be treated as being sent to either the (N/2)th data output pins or to the ((N/2)+1)th to Nth data output pins respectively.

Claim 6 is recites the limitation "the ((N/2)+1)th to Nth Data output pins" in line 3 of the claim and "the ((N/2)+1)th to Nth output signals" in line 4 of the claim. There is insufficient antecedent basis for these limitations in the claim. Examiner notes that there are not prior references to these pins or signals within the claim.

Claims 12 and 14 have the same 35 U.S.C. 112 second paragraph issues as per claims 5 and 6.

Claims 5-6 and 12-15 recite the fraction N/2 wherein N is said to be a positive integer and the fraction (N/2) is used to determine what signals are used in conjunction with what pins. It is unclear to the examiner how a fraction of a signal or a fraction of a pin is used since this fraction (N/2) used to determine what signals are used in conjunction with what pins using positive integers produces half values.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Wright (US Patent 5909450).

1. As per claim 1, Wright teaches a semiconductor integrated circuit comprising:

A plurality of data output pins (column 4 lines 14-67 and figures 1-3);

A data processing circuit to generate output signals responsive to an input signal (column 4 lines 14-67 and figures 1-4); and

An output selection circuit with at least a normal mode and a test mode (columns 3-4 lines 52-67 figures 3-4);

Where a first group of output signals are provided to a first group of data output pins in a first test cycle of the test mode (column 3 lines 52-58, 31-42, column 5 lines 10-11); and

Where a second group of output signals are provided to a second group of data output pins during a second test cycle of the test mode (column 3 lines 52-58, 31-42, column 5 lines 10-11).

2. As per claim 2, Wright teaches where the output selection circuit repeats the first and second test cycles during testing (column 3 lines 44-58).

3. As per claims 3 and 4, Wright teaches where the output selection circuit sends ith output signals (i being a positive integer) to ith or (i+1)th data output pins respectively during the first cycle of the test mode; and where the output selection circuit sends (i+1)th output signals to ith or (i+1)th output pins respectively during the second test cycle of the test mode (figure 1-3 and columns 3-4 lines 24-26).

4. As per claim 5, Wright teaches where the output selection circuit sends first to (N/2)th output signals (N being an integer) to first to (N/2)th data output pins during the first cycle of the test mode; and where the output selection circuit sends ((N/2)+1)th to Nth output signals to first to (N/2)th output pins during a second test cycle of the test mode (figure 1-3 and columns 3-4 lines 24-26).

5. As per claim 6, Wright teaches where the output selection circuit sends the first to (N/2)th output signals (N being a integer) to the ((N/2)+1)th to Nth data output pins during the first cycle of the test mode; and where the output selection circuit sends the

((N/2)+1)th to Nth output signals to the ((N/2)+1)th to Nth output pins during the second test cycle of the test mode (figure 1-3 and columns 3-4 lines 24-26).

6. As per claim 7, Wright teaches a method for outputting data during a test mode of a semiconductor integrated circuit having a plurality of data output pins, the method comprising:

Sending some output signals to a first group of the data output pins (column 3 lines 31-58 figure 1-4); and

Sending remaining output signals to the first group of the data output pins (column 3 lines 31-58).

7. As per claim 8, Wright teaches where the sending some output signals and the sending remaining output signals are repeated during a test mode (column 3 lines 44-58).

8. As per claims 9 and 10, Wright teaches where sending some output signals includes sending ith output signals (i being a positive integer or odd integer) are sent to ith data output pins (columns 3-5 lines 24-11).

9. As per claim 11, Wright teaches where sending remaining output signals includes sending (i+1)th output signals (i being a positive integer) to ith data output pins (columns 3-5 lines 24-11).

10. As per claims 12 and 13, Wright teaches where sending some output signals includes sending first to (N/2)th output signals (N being a positive integer) to first to N/2th data output pins and sending remaining output signals includes sending

((N/2)+1)th to Nth output signals are sent to the first to (N/2)th data output pins (figure 1-3 and columns 3-4 lines 24-26).

11. As per claim 14, Wright teaches where sending some output signals includes sending first to (N/2)th output signals (N being a positive integer) to the ((N/2)+1)th to Nth data output pins and sending remaining output signals includes sending ((N/2)+1)th to Nth output signals to the ((N/2)+1)th to Nth data output pins (figure 1-3 and columns 3-4 lines 24-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

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